

PATENT APPLICATION  
42390.P3275R

**Amendment to Claims**

Please amend these claims for reissue as shown below.

1(Original). A system comprising:

a processor coupled to memory by a bus, the processor having a processor core and a pad ring, the processor core having an independent power supply;

a voltage regulator providing a plurality of voltages and providing the independent power supply;

a clock signal generator providing a clock signal at a plurality of frequencies;

a state machine to coordinate voltage and clock frequency to the processor core; and

an operating system running on the processor, the operating system monitoring an application mix executing in the processor to determine a required frequency, and determining a minimum voltage at which the processor core can operate at the required frequency, wherein the operating system directs the state machine to enter a state in which the required frequency is supplied by the clock signal generator and a closest supported voltage equal to or greater than the minimum voltage is supplied by the voltage regulator.

2(Original). The system of claim 1 wherein the voltage regulator provides one of an idle voltage or a peak voltage.

3(Original). The system of claim 1 wherein the voltage regulator can provide one voltage corresponding to each frequency supported by the clock signal generator.

## PATENT APPLICATION

42390.P3275R

4(Original). A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

accepting a measure of processor core performance need of each application currently seeking access to the processor core;

accumulating each measure of processor core performance need to find total current need;

calculating a minimum frequency that will allow the processor core to meet the total current need for the time period;

selecting a lowest supported frequency equal to or greater than the minimum frequency to be a required frequency;

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring;

supplying the required frequency and the minimum supported voltage to the processor core; and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

PATENT APPLICATION  
42390.P3275R

5(Original). A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

- establishing a maximum allowable power consumption;
- finding a maximum supported frequency which will allow the processor core to remain below the maximum allowable power consumption at the minimum supported voltage;
- selecting a required frequency to be less than or equal to the maximum supported frequency;
- finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring;
- supplying the required frequency and the minimum supported voltage to the processor core; and
- dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

6(Original). The method of claim 5 wherein a required frequency less than the maximum supported frequency is selected whenever a total processor core performance need of the current application mix can be met by a lower supported frequency.

PATENT APPLICATION  
42390.P3275R

7(Five times amended). An apparatus, comprising:

a memory; and

a processor having a processor core coupled through a pad ring to the memory and including an operating system to monitor an application mix to determine a frequency and a voltage at which the core of the processor can operate in executing the application mix, the operating system to direct adjustment of the frequency and the voltage in accordance with the application mix while the pad ring operates at a constant voltage.

8(Once amended). The apparatus of claim 7, further including a voltage regulator adapted to provide an idle voltage potential level and a peak voltage level.

9(Canceled).

10(Thrice amended). The apparatus of claim 7, wherein the operating system directs a state machine to set a minimum voltage potential level at which the processor operates.

11(Original). The apparatus of claim 7, further comprising a clock signal generator adapted to provide a clock signal of at least two frequencies.

PATENT APPLICATION  
42390.P3275R

12(Twice amended). A method comprising:  
determining active applications being executed within a processor as monitored by an  
operating system;  
matching a frequency and a voltage potential to the active applications accessed in the  
processor; and  
directing a state machine to enter a state in which the frequency and the voltage potential  
are set to at least a portion of the processor in accordance with the active applications.

13(Twice Amended). The method of claim 12, further comprising changing the  
frequency and voltage potential in response to a change in the active applications executing in the  
processor.

38-61 (Canceled).

62(Once amended). The apparatus of claim 7, further comprising a state machine  
responsive to the operational load of the processor core